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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/771,023	02/03/2004	Hsiang Lan Lung	MXIC 1564-1	3519
22470	7590	08/23/2005	EXAMINER	
HAYNES BEFFEL & WOLFELD LLP P O BOX 366 HALF MOON BAY, CA 94019			WENDLER, ERIC J	
			ART UNIT	PAPER NUMBER
			2824	
DATE MAILED: 08/23/2005				

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary

Application No.

10/771,023

Applicant(s)

LUNG, HSIANG LAN

Examiner

Eric Wendler

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 19 August 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-29 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-29 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 03 February 2004 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 2/3/04 & 3/10/04.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☒ Other: Search History.

DETAILED ACTION

Drawings

1. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description: Figure 1 - WL1, WL2, WLn, and they do not include the following reference sign(s) mentioned in the description: page 8, 89. Corrected drawing sheets in compliance with 37 CFR 1.121(d), or amendment to the specification to add the reference character(s) in the description in compliance with 37 CFR 1.121(b) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the examiner does not accept the changes, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

2. **Claims 3, 5-7, 18, 20-22** are objected to because of the following informalities: the word "about" in these claims is indefinite and fails to exactly claim the subject matter that the applicant regards as the invention. Examiner suggests omitting these words and claiming the values disclosed.

3. **Claims 2 and 16** are objected to because of the following informalities: the phrase "sufficient to" in these claims is indefinite and fails to exactly claim the subject matter that the applicant regards as the invention. Examiner suggests providing numerical values which define sufficient barrier heights and thicknesses, e.g. -- a barrier height greater than 50 Angstroms and thickness greater than 50 Angstroms --.
4. **Claims 15 and 29** are objected to because of the following informalities: the scope of the phrases "one or more", "other metal oxide material", and "etc." in these claims is indefinite and fails to exactly claim the subject matter that the applicant regards as the invention.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. **Claims 1-9, 14, 17, 18-23, and 28-29 are rejected** under 35 U.S.C. 103(a) as being unpatentable over the US Patent to Sakui et al. (6,307,807) in view of the non-patent literature submitted by the applicant (Lee et al., "A Novel Structure of SiNO₂/SiN/High *k* Dielectrics, Al₂O₃ for SONOS Type Flash Memory", Extended Abstracts of the 2002 International Conference on Solid State Device and Materials, Nagoya (2002), 162-163).

With respect to claims 1 and 17, Sakui teaches, in Figure 3 and Column 11, lines 51-58, 65-67, a NAND array with a plurality of rows coupled to bit lines and

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columns coupled to word lines. Sakui also teaches, in Column 3, lines 55-60, the programming of the memory cells by E-field assisted tunneling by applying positive voltage to the gate and a low voltage to the channels. Sakui also teaches, in Figure 8, circuitry to read data from the memory cells, in the form of a data buffer. Sakui does not teach the "TROM" cell, which comprises a gate terminal, a first channel terminal, a second channel terminal and a channel region between the first and second channel terminals, a charge trapping structure over the channel region, a tunneling dielectric between the channel region and the charge trapping structure, and a blocking dielectric between the charge trapping structure and the gate terminal. Lee teaches, in sections 1 and 2, the use of both new SONOS and SANOS structures that have the structure of the TROM cell described above. It would have been obvious to one of ordinary skill in the art, at the time of the invention, to use the SONOS or SANOS structures of Lee in the memory system of Sakui in order to solve the problem of considerable charge loss due to direct tunneling in conventional SONOS cells, as mentioned in Lee, section 1.

With respect to claims 2-5 and 18-20, Sakui teaches all the claimed elements but doesn't mention anything about the barrier height and thickness of the tunneling dielectric. Lee teaches, in sections 1 and 2, that the new SONOS device has a tunneling dielectric composed of silicon dioxide, having a thickness greater than 30 Angstroms. This is a barrier height and thickness that is sufficient to prevent direct tunneling. Also, in section 3 and Figure 7, a specific example is taught where the tunneling dielectric is 40 Angstroms, which falls inside the range of 30-70 Angstroms. It would have been obvious to one of ordinary skill in the art, at the time of the invention,

to use these tunneling dielectric thicknesses to prevent direct tunneling in order to reduce the instances of charge loss, as mentioned above.

With respect to claims 6 and 21, Sakui teaches all the claimed elements but doesn't mention specific positive voltage values. Lee teaches, in section 3, that the positive voltage applied to program and erase a SONOS device can increase up to 18 volts. It would have been obvious to one of ordinary skill in the art, at the time of the invention, to apply a positive voltage of 15 volts or greater because a larger difference in the positive voltage and ground allows for more effective Fowler-Nordheim tunneling.

With respect to claims 7 and 22, Sakui further teaches, in column 1, lines 50-60, an equation that describes Fowler-Nordheim tunneling. Sakui goes on to say that tunneling begins when the electric field is 10 volts over 10 nm, or 5 volts over 5 nm. As mentioned in the above paragraph, Lee teaches the application of a high positive voltage of 15 volts or higher. In applying the equation taught by Sakui, the electric field resulting from the teaching of Lee will be 15 volts over 5 nm, or greater. It would have been obvious to one of ordinary skill in the art, at the time of the invention, to apply the well-known equation of Sakui to the positive voltage taught by Lee in order to get an electric field of 15 volts over 5 nm, or greater, in order to achieve more effective Fowler-Nordheim tunneling.

With respect to claim 8, Sakui teaches in column 1, lines 12-16, that the array of memory cells is configured as a read only memory.

With respect to claims 9 and 23, Sakui further teaches in Figure 20, and Column 12, lines 50-55, that the cells in the array have a negative threshold voltage

prior to programming. Because F-N tunneling requires a high positive voltage applied to the gate, and a low voltage applied to the channels, the threshold voltage will be negative.

With respect to claims 14 and 28-29, Sakui teaches all the claimed elements but doesn't mention a charge trapping structure comprised of silicon nitride. Lee teaches, in section 2 and Figure 1, a charge trapping structure comprised of silicon nitride. It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have a charge trapping structure comprised of silicon nitride due to its good charge trapping properties and its relation to the hole current through a tunnel oxide and the electron current through a blocking layer.

7. **Claims 10, 16, and 24 are rejected** under 35 U.S.C. 103(a) as being unpatentable over the US Patent to Sakui et al. (6,307,807) in view of the non-patent literature submitted by the applicant (Lee et al., "A Novel Structure of SiNO₂/SiN/High *k* Dielectrics, Al₂O₃ for SONOS Type Flash Memory", Extended Abstracts of the 2002 International Conference on Solid State Device and Materials, Nagoya (2002), 162-163), and further in view of the US Patent to Eitan (5,768,192).

With respect to claims 10, 16 and 24, Sakui and Lee teach all the claimed elements except the memory array is configured for one-time programming. Eitan teaches, in column 1, lines 7-10, and column 2, lines 41-46, the use of an array of memory cells configured for one-time programming, namely in a PROM, which is a one-time programmable device. It would have been obvious to one of ordinary skill in the art, at the time of the invention, to configure the memory array for one-time

programming as it reduces the production cost and allows for better endurance characteristics.

8. **Claims 11-13, 25-27 are rejected** under 35 U.S.C. 103(a) as being unpatentable over the US Patent to Sakui et al. (6,307,807) in view of the non-patent literature submitted by the applicant (Lee et al., "A Novel Structure of SiNO₂/SiN/High *k* Dielectrics, Al₂O₃ for SONOS Type Flash Memory", Extended Abstracts of the 2002 International Conference on Solid State Device and Materials, Nagoya (2002), 162-163), and further in view of the US Patent to Johnson et al. (5,343,437).

With respect to claims 11 and 25, Sakui and Lee teach all the claimed elements, as mentioned above, except for a static random access memory device and logic which accesses data stored in the array of memory cells. Johnson teaches, in column 2, lines 8-10, an integrated circuit containing both nonvolatile memory and a static random access memory array, including logic that accesses data from both memories. It would have been obvious to one of ordinary skill in the art, at the time of the invention, to connect a nonvolatile memory array to a volatile memory array for the purpose of preserving the advantages of the nonvolatile memory while enjoying the higher performance advantages of high speed volatile memories, such as SRAMS (see column 2, lines 54-57).

With respect to claims 12-13 and 26-27, Sakui and Lee teach all the claimed element, as mentioned above, except for the use of a processor in an SRAM that executes instructions. Johnson teaches, in column 6, lines 61-68, and column 7, lines 1-5, the use of a processor that executes instructions, including instructions for access

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to data stored in the nonvolatile and volatile memories and logic that comprises instructions executed by the processor. It would have been obvious to one of ordinary skill in the art, at the time of the invention, to use a processor in this manner in order to provide flexibility to update data or instructions as necessary (see column 7, lines 2-3).

9. **Claim 15 is rejected** under 35 U.S.C. 103(a) as being unpatentable over the US Patent to Sakui et al. (6,307,807) in view of the non-patent literature submitted by the applicant (Lee et al., "A Novel Structure of SiNO₂/SiN/High *k* Dielectrics, Al₂O₃ for SONOS Type Flash Memory", Extended Abstracts of the 2002 International Conference on Solid State Device and Materials, Nagoya (2002), 162-163), and further in view of the non-patent literature (Liao et al., "Process Techniques and Electrical Characterization for High-k (HfO_xN_y) Gate Dielectric in MOS Devices", Proceedings, 7th International Conference on Solid-State and Integrated Circuits Technology, Volume 1, Oct. 2004, 372-377).

With respect to claim 15, Sakui and Lee teach all the claimed elements except for a charge trapping structure comprising a metal oxide material. Liao teaches, in the abstract and section 1, a metal oxide semiconductor device having a metal oxide (HfO_x) as a charge trapping structure. It also teaches a combination with this metal oxide with nitride (HfO_xN_y) in order to reduce strain and increase reliability. It would have been obvious to one of ordinary skill in the art, at the time of the invention, to use a metal oxide as a charge trapping structure instead of silicon nitride, especially a compound comprised of both substances, as they are both widely used as charge trapping materials.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure: Hu (5,511,020), Hiura (5,586,073), Oyama (5,691,552), Lancaster (5,774,400), Pourkeramati (5,953,254), Choi (6,894,924), Yi (2001/0048612), and Yeh (2004/0130942). Hu teaches a memory cell with the same structure as the claimed cell, but the tunneling dielectric is not sufficient to stop direct tunneling. Hiura and Yeh also teach a similar cell structure that uses charge trapping. Oyama, Lancaster, Choi, and Yi teach a similar cell but not one configured for one-time programming. Pourkeramati teaches a similar cell but with thicker layers of material. When responding to this office action, applicants are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist the examiner in locating the appropriate paragraphs.

11. A shortened statutory period for response to this action is set to expire three months and zero days from the date of this letter. Failure to respond within the period for response will cause this application to become abandoned (see MPEP 710.02 (b)).

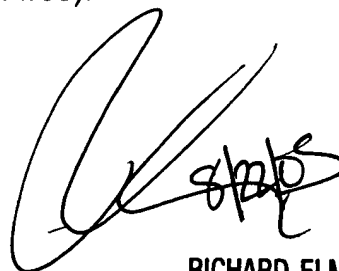
12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric Wendler whose telephone number is (571) 272-5063. The examiner can normally be reached on Monday - Friday 8 AM - 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on (571) 272-1869. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

EJW
8/19/05

A handwritten signature in black ink, appearing to read 'R. Elms', with a date '8/19/05' written below it.

RICHARD ELMS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800